

## Abstract of the Disclosure

In a precompensation circuit for magnetic recording of data signals, a clock produces clock signals at a predetermined rate to clock the recording of the data signals. A clock delay generator generates clock delay data relative to the generated clock signals for successive data signals to be recorded. The clock delay data for each data signal is formed according to the states of a set of adjacent data signals.  $n > 1$  programmable clock delay units operate sequentially to control the recording times of the successive data signals. Each clock delay unit receives the clock delay data for one data signal in each sequence of  $n$  successive data signals and determines recording time of the one data signal according to the clock delay data for the one data signal in the sequence.